



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/808,122	03/24/2004	Yue-Der Chih	N1280-00130(TSMC2003-979)	4506

7590 04/03/2006

HOWARD CHEN
PRESTON GATES & ELLIS LLP
55 SECOND STREET
SUITE 1700
San Francisco, CA 94105

EXAMINER

TON, MY TRANG

ART UNIT PAPER NUMBER

2816

DATE MAILED: 04/03/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/808,122

Applicant(s)

CHIH ET AL.

Examiner

My-Trang N. Ton

Art Unit

2816

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 11 January 2006.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-12 and 15-22 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 12 and 15-17 is/are allowed.
- 6) ☒ Claim(s) 1-6, 8-11 and 18-21 is/are rejected.
- 7) ☒ Claim(s) 7 and 22 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 24 March 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.


MY-TRANG NUTON
PRIMARY EXAMINER

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-6, 8, 10, 18-21 remain rejected under 35 U.S.C. 102(b) as being anticipated by Lall et al (U.S Patent No. 6,370,071) cited in PTOL 1449 for the reasons recited in the last Office action.

As noted in the last Office action, Lall et al discloses in Fig. 4 a high voltage CMOS switch circuit including:

Regarding claim 1: one (P2) or more transistors (P2, P4) of a same type connected in series and being operable with a normal operating voltage (EN) and a high operating voltage (Vpp);

a high operating voltage (Vpp) coupled to a first end of the device (first end coupled to P2) of the device structure (300);

a low voltage (Ground) coupled to a second end (coupled to N2); and

one (hvb) or more control voltages controllably coupled to the gates of the transistors (hvb coupled to gate of P2);

wherein at least one of the control voltages (hvb) coupled to the gate of at least one transistor (P2) is raised to a medium voltage level (Vpp – resistive loss from P1,P3) that is substantially higher than a normal operating voltage (VEN) and substantially

Art Unit: 2816

lower than the high operating voltage (V_{pp}) when operating under the high operating voltage (V_{pp}) for tolerating stress imposed thereon by the high operating voltage (due to P1, P3 have resistance values, the voltage at hvb = V_{pp} minus the resistive loss from resistive path P1, P3, thus, hvb will be substantially lower than V_{pp}).

Regarding claim 2: the medium voltage level is closer to one half of the high operating voltage (hvb = V_{pp} – the resistive loss from P1,P3 is closer to one half of the high operating voltage V_{pp} (when V_{pp} =3.3V)).

Regarding claim 3: Element N4 reads on a first NMOS transistor coupled to an output node (hv) of the structure, and element N2 reads on at least one second NMOS transistor serially coupled between the first NMOS transistor (N4) and the low voltage (Ground), the control voltage being coupled to a gate of the first NMOS transistor (N4).

Regarding claim 4: the low voltage is a ground voltage (Ground).

Regarding claim 5: Element P4 reads on a first PMOS transistor, and element P2 reads on at least one second PMOS transistor.

Regarding claim 6: the transistor have separated N wells (see P2, P4).

Regarding claim 8: the high operating voltage is above 10V (V_{pp} is pumped up to 13 volts, see col. 5, line 2-5).

Regarding claim 10: the stress is a gated stress (P2, P4).

Regarding claim 18:

a first cascade device structure (P2, P4) having one (P2) or more (P2, P4) P type transistors connected in series with one end thereof connected to the high operating voltage (P2 connected to V_{pp}); and

one (hvb) or more control voltages controllably coupled to the gates of the transistors (hvb coupled to gate of P2) in the first cascade device structure (P2) for raising voltages on one (P2) or more gates of the transistors to one or more medium values (hvb = V_{pp} – resistive loss from P1,P3) that are substantially above the normal operating voltage (EN) and substantially below the high operating voltage (V_{pp}) for tolerating voltage stress imposed by the high operating voltage (the voltage at hvb = V_{pp} – the resistive loss from resistive path P1, P3 that is higher than V_{EN} , and less than V_{pp} due to resistive loss);

wherein the P type transistors have separated N wells (see P2, P4 and col. 2, lines 52-54, and col. 5, line 66 – col. 6, line 3).

Regarding claim 19: a second cascade device structure (N4, N2) in series with the first cascade device structure (P2, P4) at its other end having one or more N type transistors (N4, N2).

Regarding claim 20: the control voltages (hvb, V_{cc} , ENB) for the first and second cascade device structure (P2, P4, N4, N2) are controlled separately depending on the input signal (EN).

Regarding claim 21: the second cascade device structure (N4, N2) is further connected to a grounding voltage (Ground).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

Art Unit: 2816

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 9 and 11 remain rejected under 35 U.S.C. 103(a) as being unpatentable over Lall et al as applied to claims 1 and 8 above.

As noted in the last Office action, this reference does not specially show "the normal operating voltage is below 2V" as recited in claim 9 and "the stress is a gated stress" as recited in claim 11.

Although Lall et al do not expressly state the value for the normal operating voltage, this difference is not of patentable merit because it is notoriously well known in the art that different values for the operating voltage can be selected in order to produce correspondingly different output values. Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to utilize the normal operating voltage EN is below 2 volts in realizing the circuit of the Lall et al reference for the purpose of producing different output values when different values of the operating voltage is selected.

Regarding the limitation "the stress is a drain stress" recited in claim 11: this appears to be obvious variations (i.e., not patentably distinct) to limitations "the stress is a gated stress". Therefore, it would have been obvious to one of ordinary skill in the art to employ (the stress is a drain stress for P2, P4), as they appear to be obvious variations (not patentably distinct) and yielding same functional device.

Allowable Subject Matter

Claims 7 and 22 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of

Art Unit: 2816

the base claim and any intervening claims. None of the prior art disclosed or suggested to show the particular structure and/or the particular operation recited in these claims namely: "the control voltages are determined so that the stress imposed by the high voltage is about equally divided by the transistors in the device structure" (claim 7); "an input module ... raised to a predetermined medium value" (claim 22).

Claims 12 and 15-17 are allowable over the prior art of record.

Response to Arguments

Applicant's arguments filed 1/11/06 have been fully considered but they are not persuasive.

Applicant's argument – hvb cannot be substantially lower than Vpp.

Examiner's response - as noted in the last Office action, because P1 and P2 of Lall have resistance values, thus, the voltage at hvb will not be equal to the high operating voltage Vpp. The voltage at hvb will be equal to Vpp minus the resistive loss from the resistive path P1, P3, thus, the limitation "substantially ... lower than the high operating voltage" is clearly met as recited in claims 1 and 18. In response to Applicant's argument regarding the limitation "substantially", under broadest reasonable interpretation, if the resistive loss is 0.7 V, then the difference between the medium voltage and the high operating voltage is large enough in amount to be noticeable (less than 1.4V). Moreover, it should be noted that the claims are not seen to require that the circuit limited to specific voltage or range (for example: how low is considered as "substantially lower") . Thus, Applicant's argument cannot be file persuasive.

Conclusion

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to My-Trang N. Ton whose telephone number is 571-272-1754. The examiner can normally be reached on 7:00 a.m - 5:30 p.m.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR.

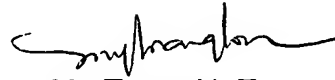
Art Unit: 2816

Status information for unpublished applications is available through Private PAIR only.

For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should

you have questions on access to the Private PAIR system, contact the Electronic

Business Center (EBC) at 866-217-9197 (toll-free).



My-Trang N. Ton
Primary Examiner
Art Unit 2816

March 28, 2006